REMARKS

In the Official Action mailed on **24 November 2008**, Examiner reviewed claims 1-2, 4-11, and 13-20. Examiner rejected claims 1, 10, and 19 under 35 U.S.C. § 103(a) based on Herlihy et al. (U.S. Patent No. 5,428,761, hereinafter "Herlihy"), in view of Callander et al. (U.S. Patent No. 5,226,150, hereinafter "Callander"). Examiner rejected claims 2, 4-7, 9, 11, 13-16, 18, and 20 under 35 U.S.C. § 103(a) based on Herlihy, Callander, and Rajwar et al. (U.S. Patent No. 7,120,762, hereinafter "Rajwar"). Examiner rejected claims 8 and 17 under 35 U.S.C. § 103(a) based on Herlihy, Callander, Rajwar, and Hecht et al. (U.S. Pub. No. 2003/0064808, hereinafter "Hecht").

Interview Summary

In a telephone interview conducted on **05 January 2009**, Applicant discussed claim amendments to overcome prior rejections. Specifically, Applicant discussed the distinction between the store buffer of embodiments of the present invention and the Herlihy system. In response to the interview, Applicant submits the following amendments.

Rejections under 35 U.S.C. 103(a)

Examiner rejected claims 1, 10, and 19 under 35 U.S.C. § 103(a) based on Herlihy in view of Callander. Applicant respectfully disagrees. Neither Herlihy nor Callander, either separately or combined, disclose placing transactional stores in a store buffer in the processor during the transaction, wherein the transactional stores are gated and not committed to memory during the transaction.

Herlihy discloses a computer system which includes a CPU and a cache memory separate from the CPU (see Herlihy, FIG. 1; also col. 5, lines 28-33). The Herlihy system uses a transaction bit and a status bit to facilitate transactional

operations (see Herlihy, col. 6, lines 29-38). When the Herlihy CPU has finished processing data for a transaction, the CPU writes the result to the cache (see Herlihy, col. 6, lines 53-56). Then, when the transaction ends, if the status bit is still set, the Herlihy CPU commits the result to memory (see Herlihy, col. 6, lines 62-68). To assist the Examiner, Applicant respectfully quotes from Herlihy:

> When the CPU 10 has finished its alteration of the location A data in its internal register set, **it writes the result to cache 15**, and is ready to end the transaction; the CPU first checks the status bit 26 (i.e., a "commit" operation as described below). If it finds the status bit 26 reset, the transaction is scrubbed, and begins again. That is, the CPU 10 will again read the value at location A into its cache 15, set the status bit 26 and transaction bit 25, and do the updating of the counter value as before. Whenever it completes its activity on the value from location A and finds the status bit 26 still set, the CPU **makes the transaction visible to the other users of the memory 12 by clearing the transaction bit 25 and allowing a write back from cache 15 to memory 12 if another CPU 13 sends a read or write request for location A onto the bus 11** (see Herlihy, col. 6, lines 53-68, emphasis added).

In other words, the Herlihy system *always* writes the result of a transactional operation to the cache, but does not *release the cache line to other processors* until the transaction is complete. Herlihy nowhere discloses placing transactional stores in a store buffer **in the processor** during the transaction, wherein the transactional stores are gated and **not committed to memory** from the store buffer during the transaction. Moreover, Collander nowhere discloses this limitation.

In contrast, embodiments of the present invention include a store buffer **in the processor** that is a hardware structure separate from the caches in the computer system (see instant application, par. [0052]; also, FIG. 1). During a transaction, embodiments of the present invention place store data from stores in the store buffer, but not in the caches (see instant application, par. [0074]). Store data remains in the store buffer and is **not committed to memory during the**

transaction (see instant application, par. [0069] and par. [0074]). Instead, in embodiments of the present invention store data can be committed to memory during a commit operation (see instant application, par. [0079]; also, FIG. 7).

The Herlihy system is fundamentally distinct from embodiments of the present invention, because in the Herlihy system the cache line is *always* written to the cache, which is separate from the Herlihy CPU. In contrast to Herlihy, the claimed invention holds stores in a store buffer in the processor until the transaction is committed. A person skilled in the art will recognize that embodiments of the present invention can preserve bandwidth for the memory system by holding the data in the store buffer during a transaction. In addition, embodiments of the present invention can enable simpler recovery in the event of transactional failure because all of the held stores can be invalidated in the store buffer (see instant application, par. [0081]).

Accordingly, Applicant has amended the independent claims to clarify that embodiments of the present invention place transactional stores in a store buffer **in the processor** during the transaction, wherein the transactional stores are gated and **not committed to memory** from the store buffer during the transaction. These amendments are supported in par. [0052], pars. [0062]-[0079], and FIG. 1 of the instant application. No new matter was added. Neither Herlihy nor Callander, either separately or combined, disclose placing transactional stores in a store buffer in the processor during the transaction, wherein the transactional stores are gated and not committed to memory from the store buffer during the transaction.

Hence, Applicant respectfully submits that independent claims 1, 10, and 19 as presently amended are in condition for allowance. Applicant also submits that the dependent claims that depend upon these independent claims are in condition for allowance and for reasons of the unique combinations recited in such claims.

CONCLUSION

It is submitted that the application is presently in form for allowance. Such action is respectfully requested.

Respectfully submitted,

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